NIPPON PRECISION CIRCUITS LTD.

SM5841A/B

Audio Multi-function Digital Filter

OVERVIEW

The SM5841A/B are digital filters for digital audio, fabricated in Molybdenum-gate CMOS.

The SM5841A/B feature selectable digital de-emphasis digital attenuation and soft mute functions. The serial data format uses 16-bit input words and 16-, 18- or 20-bit output words. They can operate from a standard 5 V supply or a low-voltage 3.2 V supply.

The SM5841A/B are available in 22-pin SOPs and 18-pin plastic DIPs.

FEATURES

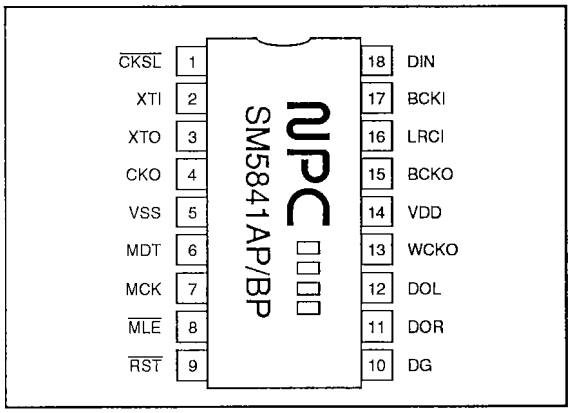
- Filter configuration
  - 2-channel, 4-times or 8-times oversampling (interpolation) filter
  - 3-stage interpolation (69-tap + 13-tap + 9-tap)
  - IIR deemphasis filter for accurate gain and phase response
  - Digital attenuator
  - Overflow limiter
  - Crystal oscillator
- Filter characteristics (fs = sampling frequency)
  - 0.20 ±0.03 dB passband (0 to 0.4535fs) ripple
  - 53 dB (min) stopband attenuation (0.5465fs to 7.4535fs in 8fs mode and 0.5465fs to 3.4535fs in 4fs mode)
  - Linear phase (zero group delay)
- Input/output
  - 16-bit serial data input (2s-complement, MSB-first, normal/IIS selectable)
  - 16-, 18- or 20-bit serial data output (4fs L/R alternating or 8fs L/R simultaneous, 2s-complement, MSB-first, stereo/bilingual mode select)
  - DC offset (approximately 0.8%) correction (SM5841B only)
  - TTL-compatible
- 256fs/384fs system clock selectable
- Supply voltage
  - 5 V normal-voltage operation
  - 3.2 V low-voltage operation
- 18-pin plastic DIP or 22-pin SOP
- Molybdenum-gate CMOS process
- Filter functions
  - 1st-order noise shaper (ON/OFF selectable)
  - Soft muting
  - Digital attenuation
  - Digital deemphasis (for 32, 44.1 and 48 kHz)

APPLICATIONS

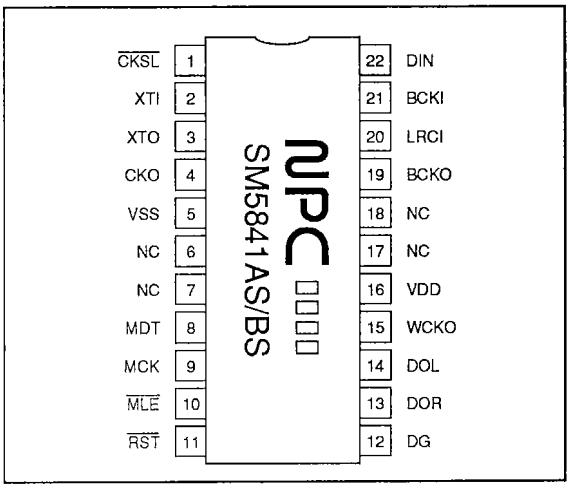
- CD playback systems
- DAT playback systems
- PCM playback systems

PINOUTS

18-pin DIP



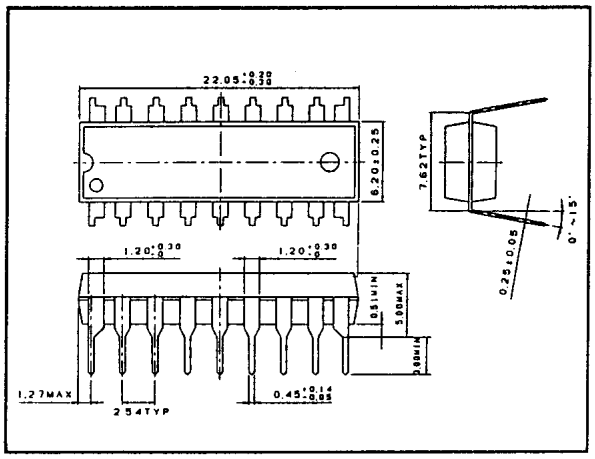
22-pin SOP



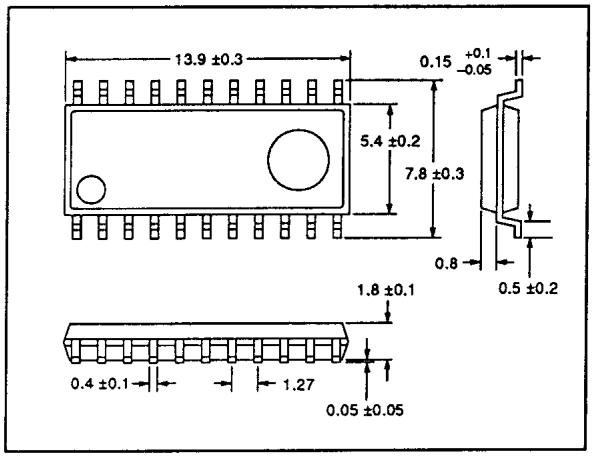
PACKAGE DIMENSIONS

Unit: mm

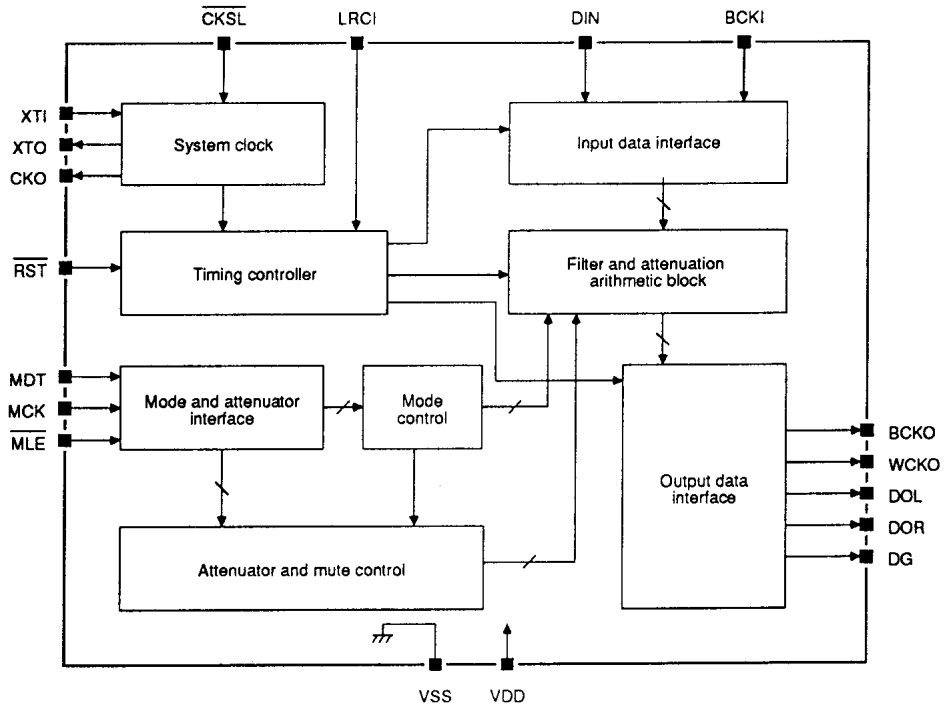
18-pin DIP



22-pin SOP



BLOCK DIAGRAM



PIN DESCRIPTION

Number		Name	I/O	Description
SOP	DIP			
1	1	$\overline{\text{CKSL}}$	ip	Oscillator and input frequency select. 384fs when HIGH, and 256fs when LOW.
2	2	XTI	i	Oscillator input connection
3	3	XTO	o	Oscillator output connection
4	4	CKO	o	Oscillator output clock (same frequency as XTI)
5	5	VSS		Ground

Number		Name	I/O	Description
SOP	DIP			
6	–	NC		No connection
7	–	NC		No connection
8	6	MDT	ip	Digital attenuator and mode set data
9	7	MCK	ip	Digital attenuator and mode set clock
10	8	$\overline{MLE}$	ip	Digital attenuator and mode set latch enable
11	9	$\overline{RST}$	ip	System reset
12	10	DG	o	8fs left/right simultaneous or 4fs left/right alternating de-glitched output
13	11	DOR	o	Right-channel data output when in 8fs L/R simultaneous mode, and LR clock output in 4fs L/R alternating mode.
14	12	DOL	o	Left-channel data output when in 8fs L/R simultaneous mode, and left/right-channel data output in L/R alternating mode.
15	13	WCKO	o	Output word clock
16	14	VDD		5 V supply
17	–	NC		No connection
18	–	NC		No connection
19	15	BCKO	o	Output bit clock
20	16	LRCI	ip	Input data sample rate (fs) clock
21	17	BCKI	ip	Input bit clock
22	18	DIN	ip	Data input

Note

i = input, ip = input with pull-up resistance, o = output

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	–0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	250	mW
Storage temperature range	T_{stg}	–40 to 125	deg. C
Soldering temperature	T_{sld}	255	deg. C
Soldering time	t_{sld}	10	s

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	3.2 to 5.5	V
Operating temperature range	T_{opr}	–20 to 80	deg. C

DC Electrical Characteristics

Normal-voltage mode

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 deg. C unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply current	I_{DD}	V_{DD} = 5.0 V, f_{SYS} = 256fs = 13 MHz, no load	–	–	40	mA
XTI HIGH-level input voltage	V_{IH1}		0.7V_{DD}	–	–	V
XTI LOW-level input voltage	V_{IL1}		–	–	0.3V_{DD}	V
HIGH-level input voltage	V_{IH2}	See note 1.	2.4	–	–	V
LOW-level input voltage	V_{IL2}		–	–	0.5	V
HIGH-level output voltage	V_{OH}	I_{OH} = –0.4 mA. See note 2.	2.5	–	–	V
LOW-level output voltage	V_{OL}	I_{OL} = 1.6 mA. See note 2.	–	–	0.4	V
XTI HIGH-level input leakage current	I_{LH}	V_{IN} = V_{DD}	–	10	20	µA
XTI LOW-level input leakage current	I_{LL}	V_{IN} = 0 V	–	10	20	µA
HIGH-level input leakage current	I_{LH}	V_{IN} = V_{DD}. See note 1.	–	–	1.0	µA
LOW-level input current	I_{IL}	V_{IN} = 0 V. See note 1.	–	10	20	µA

Notes

1. Pins LRCI, DIN, BCKI, $\overline{\text{CKSL}}$, MDT, MCK, $\overline{\text{MLE}}$ and $\overline{\text{RST}}$
2. Pins CKO, DOL, DOR, BCKO, WCKO and DG

Low-voltage mode

V_{DD} = 3.2 to 4.5 V, V_{SS} = 0 V, T_a = –20 to 70 deg. C unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply current	I_{DD}	V_{DD} = 3.4 V, f_{SYS} = 256fs = 11.5 MHz, no load	–	–	20	mA
XTI HIGH-level input voltage	V_{IH1}		0.7V_{DD}	–	–	V
XTI LOW-level input voltage	V_{IL1}		–	–	0.3V_{DD}	V
HIGH-level input voltage	V_{IH2}	See note 1.	2.4	–	–	V
LOW-level input voltage	V_{IL2}		–	–	0.5	V
HIGH-level output voltage	V_{OH}	I_{OH} = –0.2 mA. See note 2.	2.5	–	–	V
LOW-level output voltage	V_{OL}	I_{OL} = 0.8 mA. See note 2.	–	–	0.4	V
XTI HIGH-level input leakage current	I_{LH}	V_{IN} = V_{DD}	–	–	12	µA

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
XTI LOW-level input leakage current	I_{LL}	V_{IN} = 0 V	–	–	12	µA
HIGH-level input leakage current	I_{LH}	V_{IN} = V_{DD}. See note 1.	–	–	1.0	µA
LOW-level input current	I_{IL}	V_{IN} = 0 V. See note 1.	–	–	12	µA

Notes

1. Pins LRCI, DIN, BCKI, $\overline{\text{CKSL}}$, MDT, MCK, $\overline{\text{MLE}}$ and $\overline{\text{RST}}$
2. Pins CKO, DOL, DOR, BCKO, WCKO and DG

AC Electrical Characteristics

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 deg. C for normal-voltage operation.
V_{DD} = 3.2 to 4.5 V, V_{SS} = 0 V, T_a = –20 to 70 deg. C for low-voltage operation.
Typical values are measured at fs = 44.1 kHz.

System clock

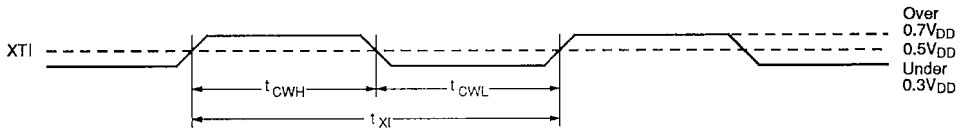
Crystal oscillator operation

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Oscillator frequency	f_{MAX}	384fs, $\overline{\text{CKSL}}$ = HIGH	4.0	16.9	19.3	MHz
		256fs, $\overline{\text{CKSL}}$ = LOW	4.0	11.3	13.0	

External clock input operation

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
XTI HIGH-level clock pulsewidth	t_{CWH}	384fs, $\overline{\text{CKSL}}$ = HIGH	21.7	29.5	125	ns
		256fs, $\overline{\text{CKSL}}$ = LOW	34	44.3	125	
XTI LOW-level clock pulsewidth	t_{CWL}	384fs, $\overline{\text{CKSL}}$ = HIGH	21.7	29.5	125	ns
		256fs, $\overline{\text{CKSL}}$ = LOW	34	44.3	125	
XTI clock pulse time	t_{XI}	384fs, $\overline{\text{CKSL}}$ = HIGH	51.7	59.0	250	ns
		256fs, $\overline{\text{CKSL}}$ = LOW	77	88.6	250	

System clock timing waveform

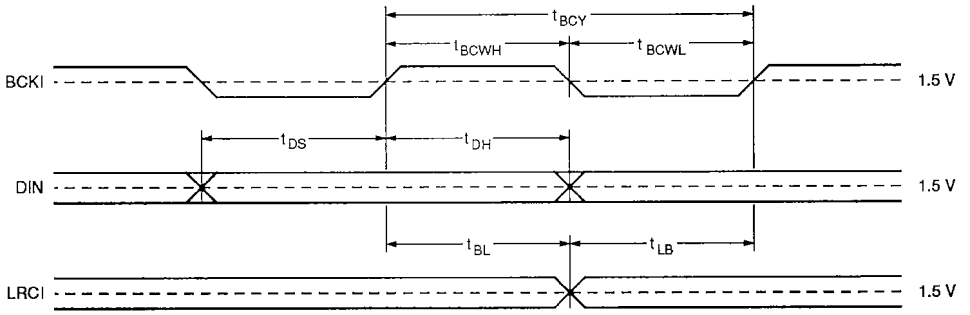


Serial input timing (BCKI, DIN, LRCI)

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKI HIGH-level pulsewidth	t_{BCWH}	50	–	–	ns
BCKI LOW-level pulsewidth	t_{BCWL}	50	–	–	ns

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKI pulse period	t_{BCY}	100	–	–	ns
DIN setup time	t_{DS}	50	–	–	ns
DIN hold time	t_{DH}	50	–	–	ns
Last BCKI rising edge to LRCI edge	t_{BL}	50	–	–	ns
LRCI edge to first BCKI rising edge	t_{LB}	50	–	–	ns

BCKI, DIN and LRCI input timing waveform



Reset timing

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
$\overline{RST}$ LOW-level pulsewidth	t_{RST}	At power-on	1	–	–	µs
		At other times	50	–	–	ns

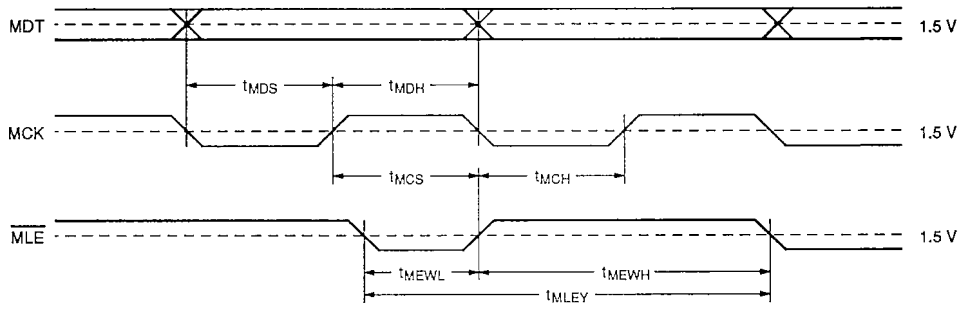
Control input timing (MDT, MCK, $\overline{MLE}$)

Parameter	Symbol	Rating			Unit
		min	typ	max	
MDT setup time	t_{MDS}	40	–	–	ns
MDT hold time	t_{MDH}	40	–	–	ns
$\overline{MLE}$ setup time	t_{MCS}	60	–	–	ns
$\overline{MLE}$ hold time	t_{MCH}	40	–	–	ns
$\overline{MLE}$ LOW-level pulsewidth	t_{MEWL}	40	–	–	ns
$\overline{MLE}$ HIGH-level pulsewidth	t_{MEWH}	40	–	–	ns
$\overline{MLE}$ pulse interval	t_{MLEY}	6	–	–	t_{SYS}
MCK and $\overline{MLE}$ rise time	t_r	–	–	100	ns
MCK and $\overline{MLE}$ fall time	t_f	–	–	100	ns

Note

t_{SYS} = system clock cycle time (1/384fs when $\overline{CKSL}$ = HIGH and 1/256fs when $\overline{CKSL}$ = LOW)

Control input timing waveform



Output timing

Normal-voltage mode

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Oscillator input to output delay	t_{XTO}	XTI falling edge to XTO rising edge	3	–	20	ns
Oscillator input to clock output delay	t_{CKO}	XTI falling edge to CKO falling edge	7	–	30	ns
Oscillator input to bit clock output delay ($\overline{CKSL}$ = HIGH)	t_{sbH}	XTI falling edge to BCKO rising edge	10	–	60	ns
	t_{sbL}	XTI falling edge to BCKO falling edge	10	–	60	ns
Oscillator input to bit clock output delay ($\overline{CKSL}$ = LOW)	t_{sbH}	XTI rising edge to BCKO rising edge	10	–	60	ns
	t_{sbL}	XTI falling edge to BCKO falling edge	10	–	60	ns
Bit clock output to data output and word clock output delay	t_{bdH1}	BCKO falling edge to rising-edge output	0	–	20	ns
	t_{bdL1}	BCKO falling edge to falling-edge output	0	–	20	ns
Bit clock output to de-glitched output delay	t_{bdH2}	BCKO rising edge to rising-edge output	0	–	20	ns
	t_{bdL2}	BCKO rising edge to falling-edge output	0	–	20	ns

Notes

All measurements with 15 pF load

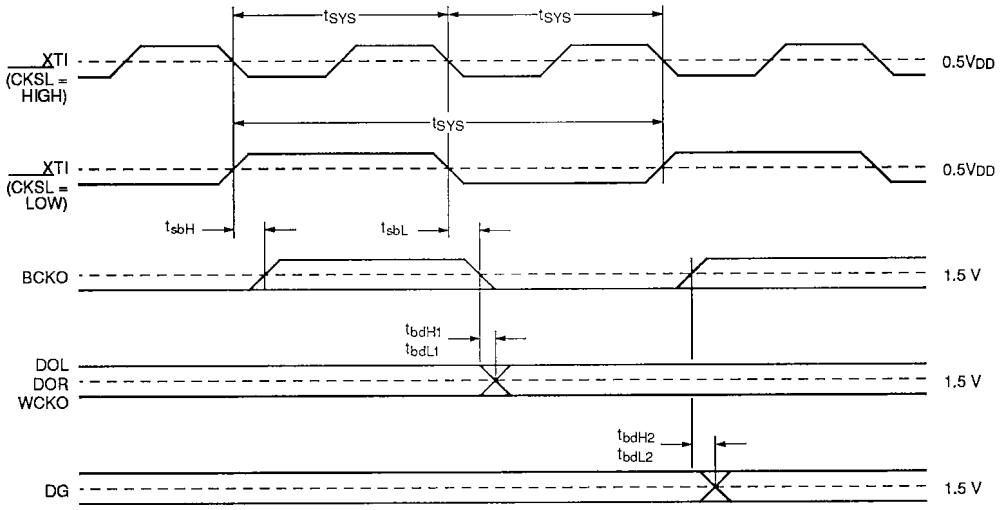
Low-voltage mode

V_{DD} = 3.2 to 4.5 V, V_{SS} = 0 V, T_a = –20 to 70 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Oscillator input to output delay	t_{XTO}	XTI falling edge to XTO rising edge	3	–	30	ns
Oscillator input to clock output delay	t_{CKO}	XTI falling edge to CKO falling edge	7	–	45	ns
Oscillator input to bit clock output delay ($\overline{CKSL}$ = HIGH)	t_{sbH}	XTI falling edge to BCKO rising edge	10	–	100	ns
	t_{sbL}	XTI falling edge to BCKO falling edge	10	–	100	ns
Oscillator input to bit clock output delay ($\overline{CKSL}$ = LOW)	t_{sbH}	XTI rising edge to BCKO rising edge	10	–	100	ns
	t_{sbL}	XTI falling edge to BCKO falling edge	10	–	100	ns
Bit clock output to data output and word clock output delay	t_{bdH1}	BCKO falling edge to rising-edge output	0	–	30	ns
	t_{bdL1}	BCKO falling edge to falling-edge output	0	–	30	ns
Bit clock output to de-glitched output delay	t_{bdH2}	BCKO rising edge to rising-edge output	0	–	30	ns
	t_{bdL2}	BCKO rising edge to falling-edge output	0	–	30	ns

Notes
All measurements with 15 pF load

Output timing waveform



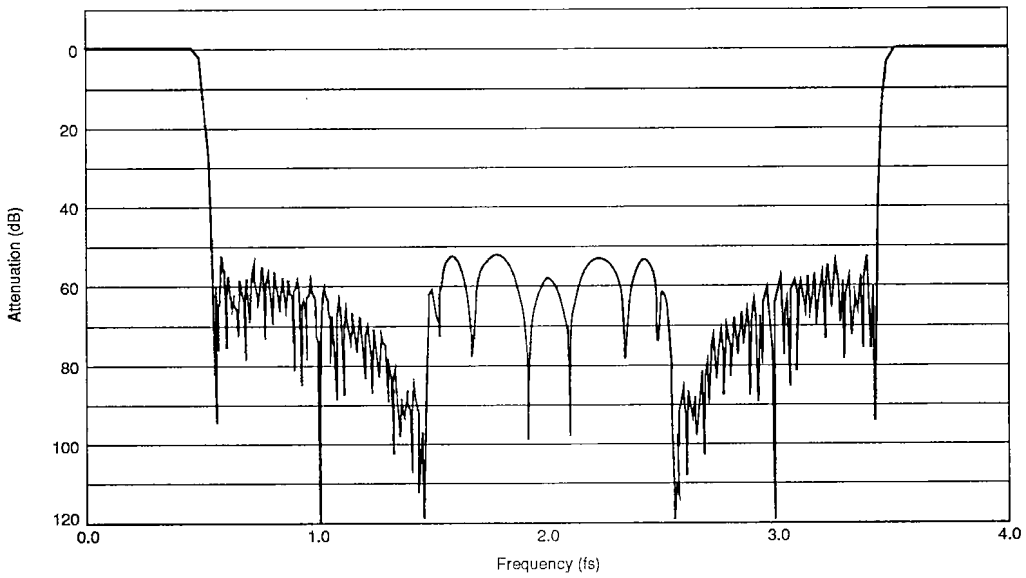
Note
The output timing shows the timing relationship between DOL/DOR/WCKO/DG and XTI and BCKO. It does not show the timing relationship between outputs.

Filter Characteristics

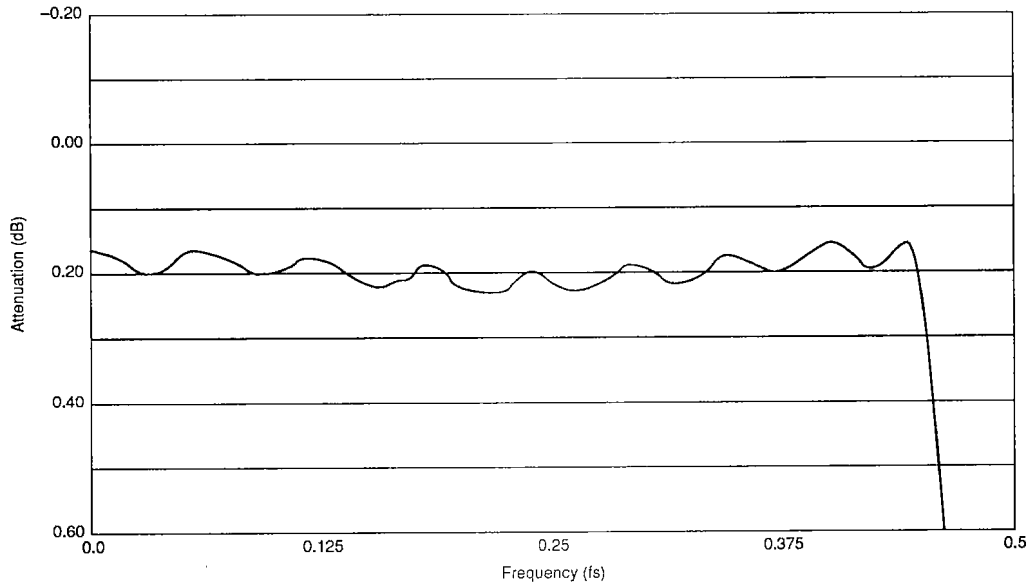
SM5841A 4-times interpolation filter

Parameter	Frequency		Rating (dB)		
	f	@fs = 44.1 kHz	min	typ	max
Passband attenuation	0 to 0.4535fs	0 to 20 kHz	–	0.20	–
Passband ripple			–0.03	–	0.03
Stopband attenuation	0.5465fs to 3.4535fs	24.1 to 152 kHz	53	–	–

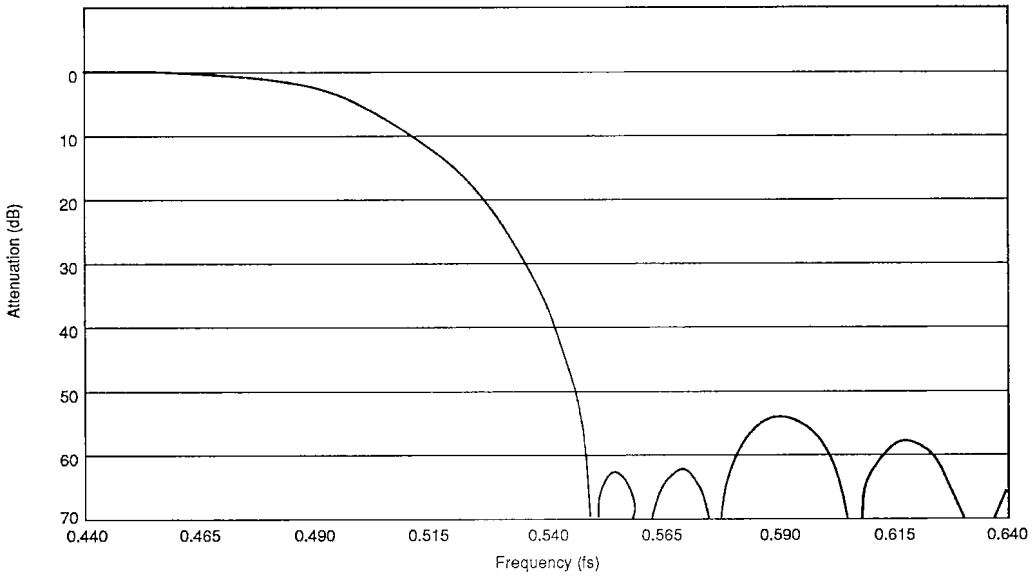
4fs filter frequency characteristic (Deemphasis OFF)



4fs filter passband characteristic (Deemphasis OFF)



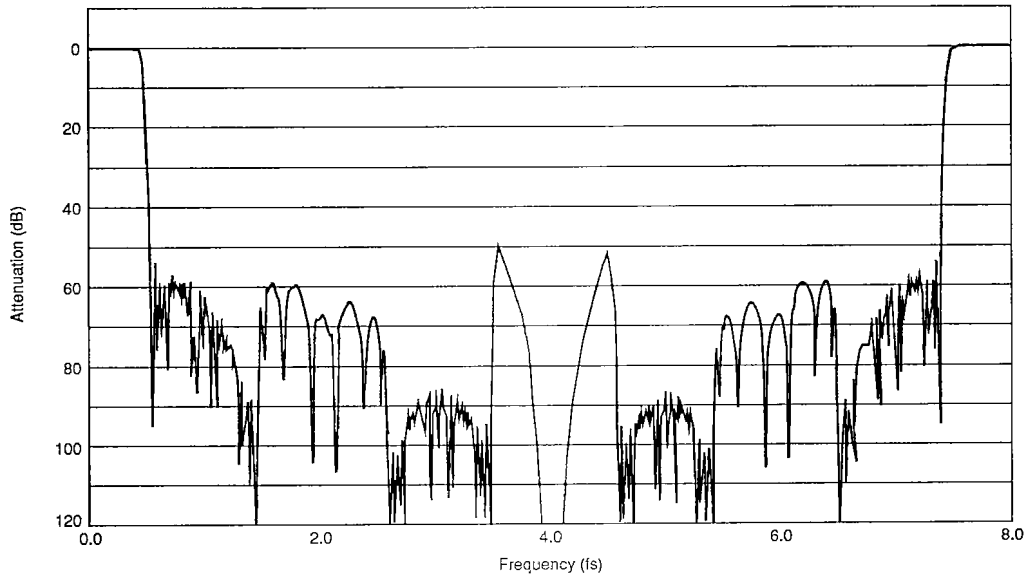
4fs filter band-transition characteristic (Deemphasis OFF)



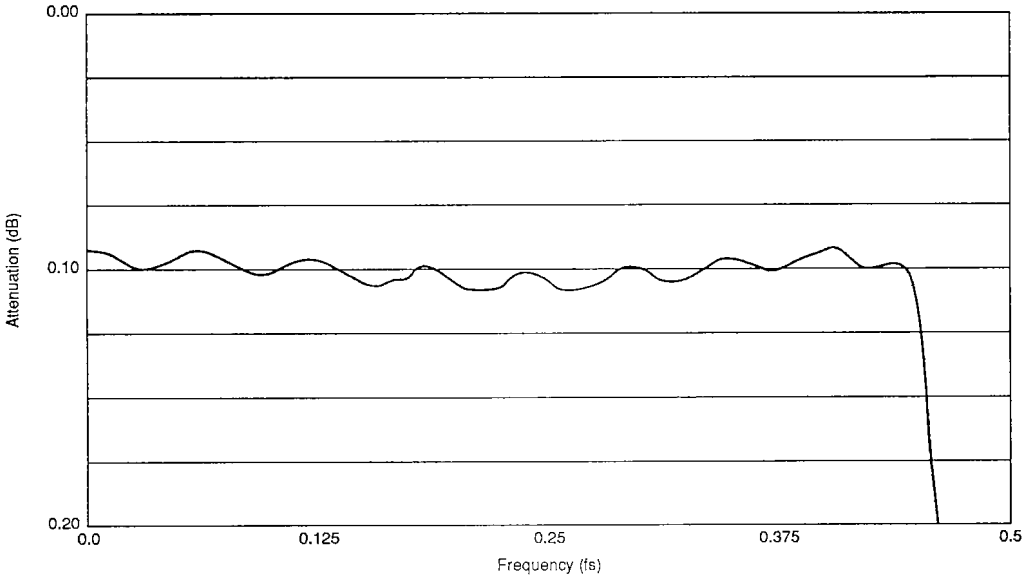
SM5841A 8-times interpolation filter

Parameter	Frequency		Rating (dB)		
	f	@fs = 44.1 kHz	min	typ	max
Passband attenuation	0 to 0.4535fs	0 to 20 kHz	–	0.20	–
Passband ripple			–0.03	–	0.03
Stopband attenuation	0.5465fs to 3.4535fs	24.1 to 152 kHz	53	–	–
	3.4535fs to 4.5465fs	152 to 201 kHz	50	–	–
	4.5465fs to 7.4535fs	201 to 328 kHz	53	–	–

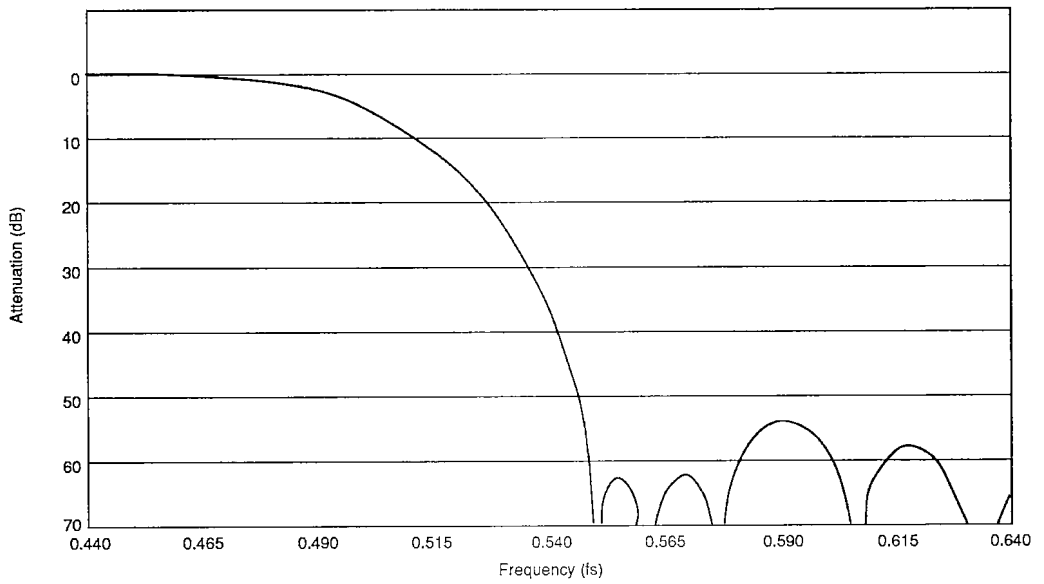
8fs filter frequency characteristic (Deemphasis OFF)



8fs filter passband characteristic (Deemphasis OFF)



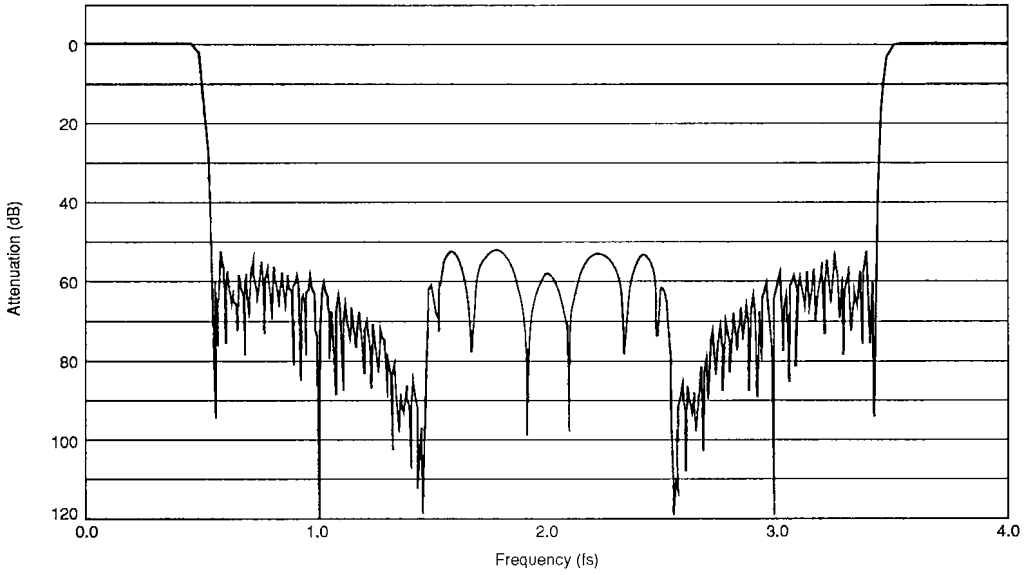
8fs filter band-transition characteristic (Deemphasis OFF)



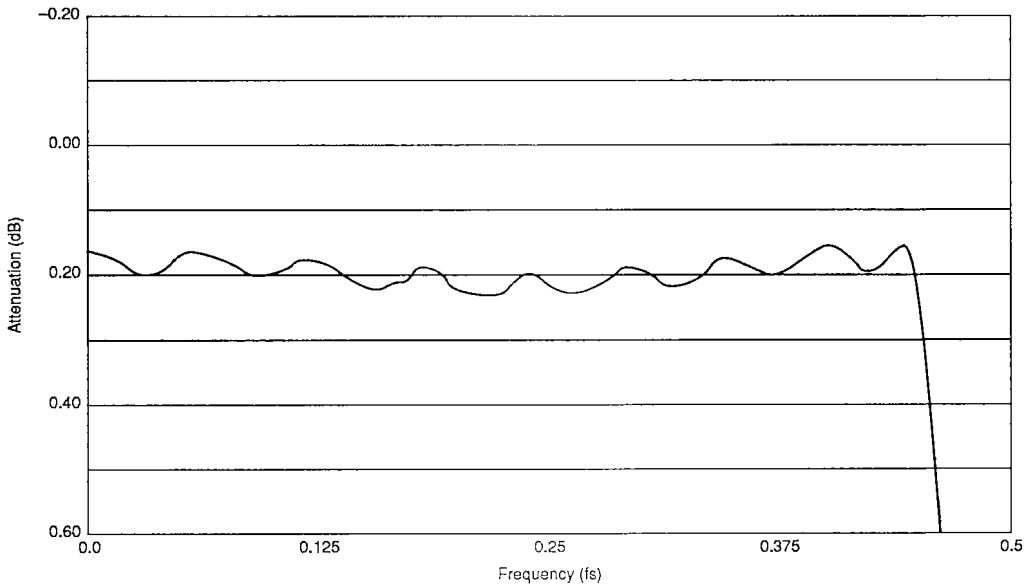
SM5841B 4-times interpolation filter

Parameter	Frequency		Rating (dB)		
	f	@fs = 44.1 kHz	min	typ	max
Passband attenuation	0 to 0.4535fs	0 to 20 kHz	–	0.20	–
Passband ripple			–0.03	–	0.03
Stopband attenuation	0.5465fs to 3.4535fs	24.1 to 152 kHz	53	–	–

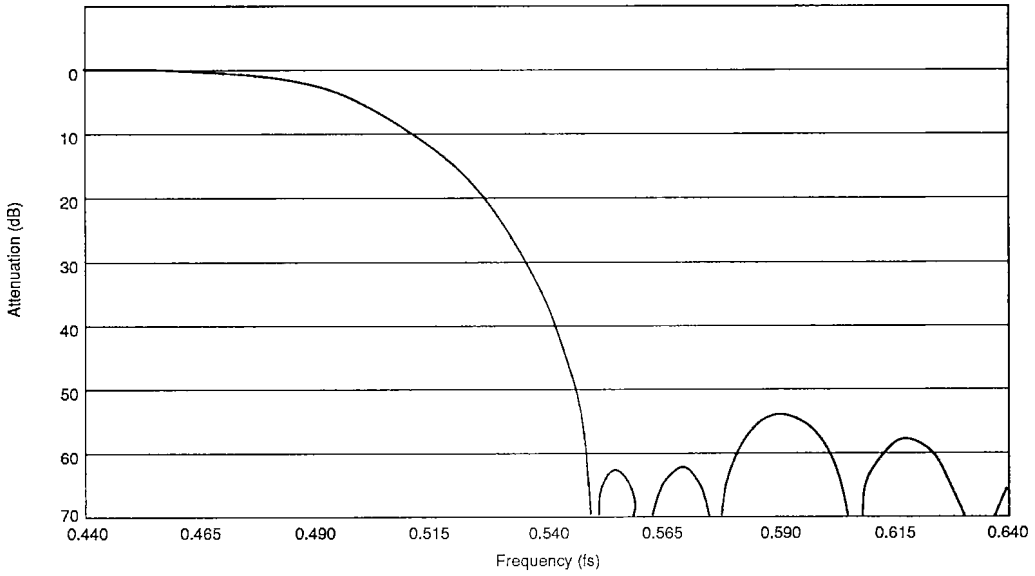
4fs filter frequency characteristic (Deemphasis OFF)



4fs filter passband characteristic (Deemphasis OFF)



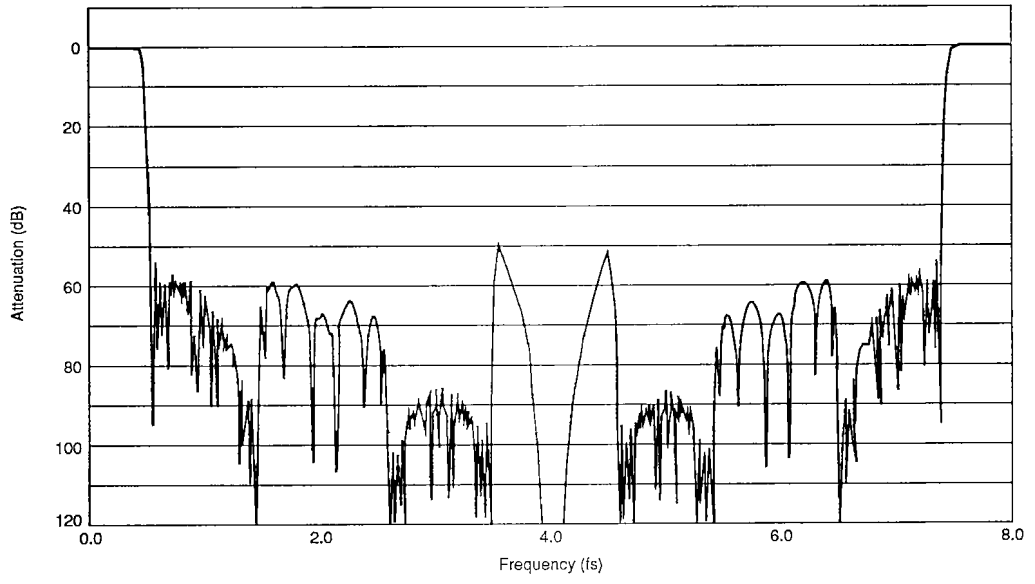
4fs filter band-transition characteristic (Deemphasis OFF)



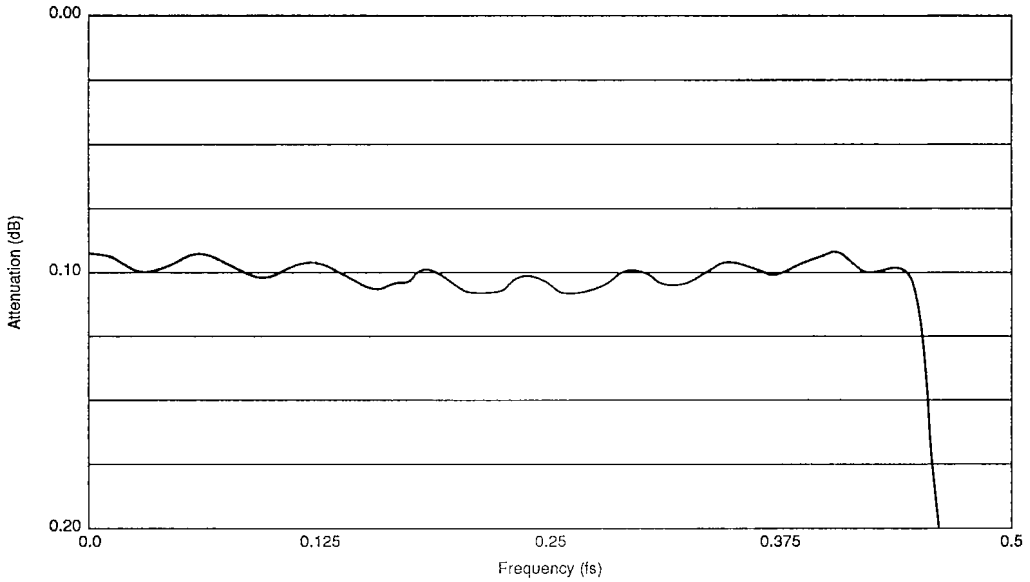
SM5841B 8-times interpolation filter

Parameter	Frequency		Rating (dB)		
	f	@fs = 44.1 kHz	min	typ	max
Passband attenuation	0 to 0.4535fs	0 to 20 kHz	–	0.20	–
Passband ripple			–0.03	–	0.03
Stopband attenuation	0.5465fs to 3.4535fs	24.1 to 152 kHz	53	–	–
	3.4535fs to 4.5465fs	152 to 201 kHz	50	–	–
	4.5465fs to 7.4535fs	201 to 328 kHz	53	–	–

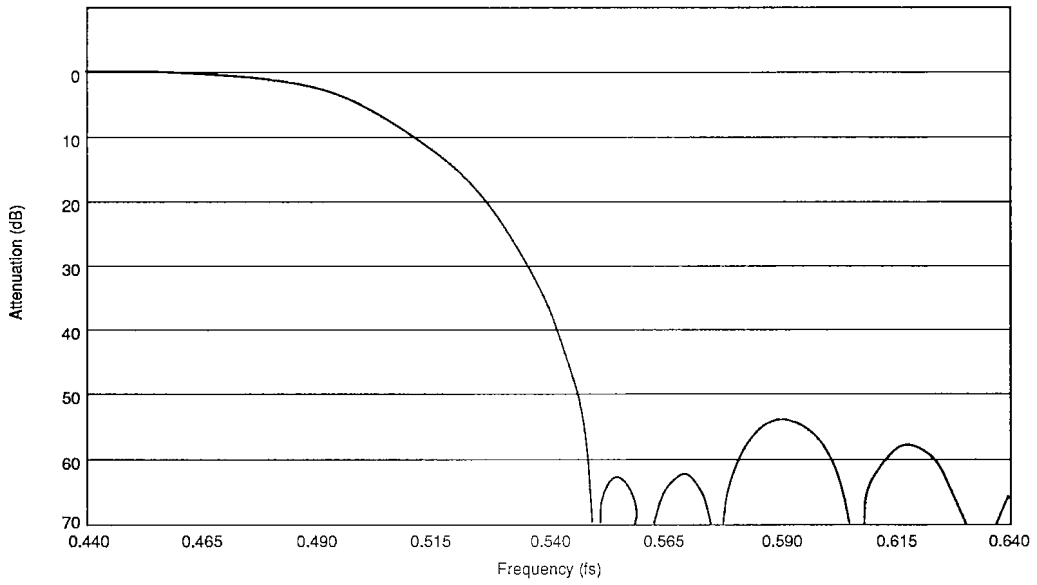
8fs filter frequency characteristic (Deemphasis OFF)



8fs filter passband characteristic (Deemphasis OFF)



8fs filter band-transition characteristic (Deemphasis OFF)

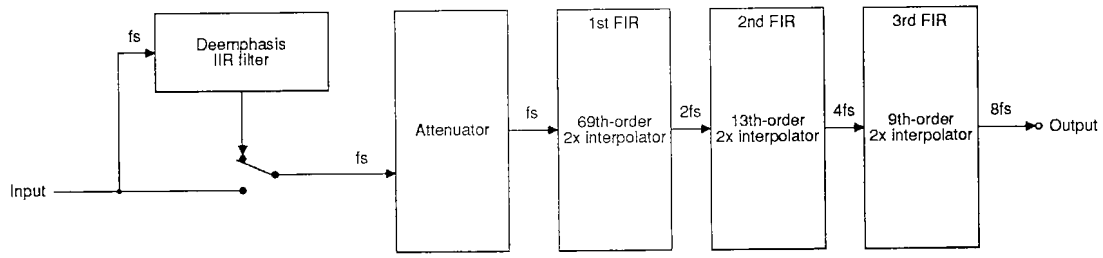


Deemphasis filter

Parameter		Sampling frequency (fs)		
		32 kHz	44.1 kHz	48 kHz
Passband bandwidth (kHz)		0 to 14.5	0 to 20.0	0 to 21.7
Deviation from ideal characteristics	Attenuation (dB)	–0.40 to 0.35	–0.05 to 0.15	–0.30 to 0.05
	Phase, θ (°)	–2 to 19	–1 to 15	–1 to 14

FUNCTIONAL DESCRIPTION

SM5841A/B Arithmetic Block



Oversampling (Interpolation)

The SM5841A/B performs oversampling using a three-stage FIR interpolation filter. Each filter stage interpolates the signal by a factor of two, giving an overall interpolation factor of eight. Sampling noise components are attenuated by the interpolation filter to greater than 53 dB in the 0.5465fs to 7.4535fs (8fs mode) and 0.5465fs to 3.4535fs (4fs mode) stopband.

Digital Deemphasis

The deemphasis filter is in cascade with the oversampling filters. It is implemented using an IIR filter, and reproduces the deemphasis gain and phase characteristics more faithfully than conventional analog deemphasis filters. Deemphasis is enabled when DEEM is HIGH, and disabled when DEEM is LOW. After initialization (system reset), deemphasis is OFF.

The filter coefficients change according to the selected sampling frequency, fs.

FSEL1	FSEL2	Sampling frequency
LOW	LOW	44.1 kHz
LOW	HIGH	48 kHz
HIGH	LOW	44.1 kHz
HIGH	HIGH	32 kHz

After initialization (system reset), 44.1 kHz sampling frequency is selected.

Digital Attenuator (MDT, MCK, $\overline{\text{MLE}}$)

The digital attenuator is used for the attenuation and mute functions. An external attenuation coefficient is loaded into an attenuation register using MDT, MCK and $\overline{\text{MLE}}$, as shown in figure 1.

The 7-bit attenuation level set data is input on MDT (MSB = LOW), MSB-first and clocked on the falling edge of MCK.

Both the left and right channels are attenuated simultaneously by an amount

$$\text{Attenuation} = 20 \times \log_{10}(1 - \text{DATT}/127)\ \text{dB}$$

where DATT is the contents of the attenuation register. When DATT = 127, the attenuation is infinite (mute function). The register is reset to 0 at system reset.

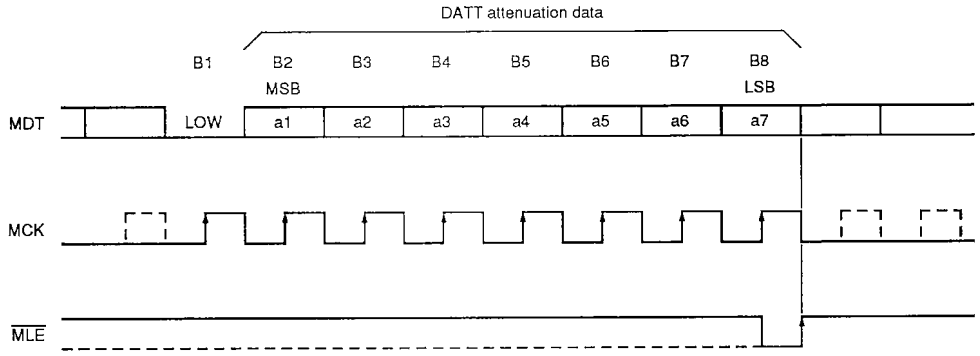


Figure 1. Attenuation data

When a new DATT attenuation coefficient is loaded, the attenuation ramps up or down to the level set by the new coefficient as shown in figure 2. If another attenuation coefficient is loaded before this new level is reached, the gain ramps in the direction of the latest set level. This occurs because coefficents are temporarily stored in a different register.

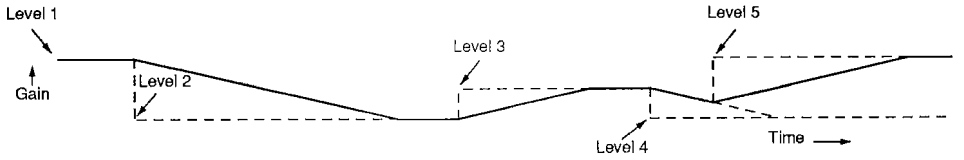


Figure 2. Attenuation level changes

Soft Mute

The oversampled output can be muted using the MUTE flag. Muting is ON when MUTE is HIGH, and OFF when MUTE is LOW.

When MUTE is HIGH, the maximum attenuation coefficient 127 is loaded into the temporary-storage register and the attenuation slowly changes to ∞ dB.

When MUTE is LOW, the value in the temporary-storage register is the value just before MUTE went LOW. If the external attenuation coefficient changes, the attenuation slowly changes to that new value.

The time taken to increase the attentuation from 0 (DATT = 1) to ∞ dB (DATT = 127) is approximately 1024/fs, which is approximately 23.2 ms at fs = 44.1 kHz.

Muting is set to OFF at system reset.

System Clock (XTI, XTO, CKO, $\overline{\text{CKSL}}$)

The system clock has 256fs and 384fs selectable frequencies. The clock can be generated either externally (input on XTI) or internally (crystal oscillator between XTI and XTO).

The clock is output on CKO, where the frequency is set by the level on $\overline{\text{CKSL}}$ as shown in table 1.

Table 1. System clock select

$\overline{\text{CKSL}}$	Clock frequency	Clock input
LOW	256fs	External clock on XTI OR Crystal oscillator between XTI and XTO
HIGH	384fs	

Mode Flags (MDT, MCK, $\overline{\text{MLE}}$)

The mode flags are set by data on the serial data interface pins (MDT, MCK and $\overline{\text{MLE}}$).

Mode flag data on MDT is clocked on the falling edge of MCK, and then shifted in a shift register on the rising edge of MCK. Data should, therefore, change on the falling edge of MCK.

The input data in the internal SIPO (serial-in, parallel-out register) is latched into the mode register on the rising edge of the $\overline{\text{MLE}}$ latch enable. Therefore, data preceding the 8-bit input should be set to 1 (HIGH).

The mode flags set are selected by the state of B1 and B2.

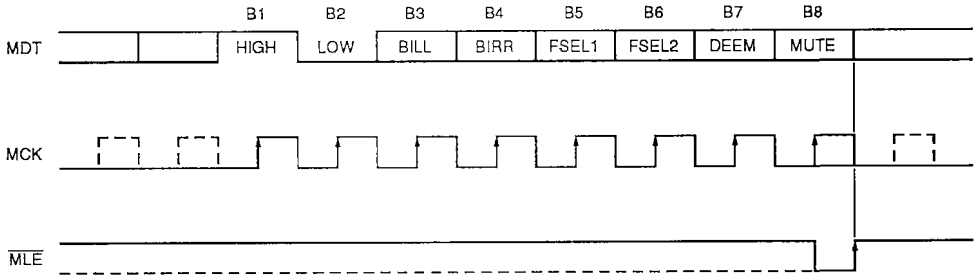


Figure 3. Mode flag setting 1

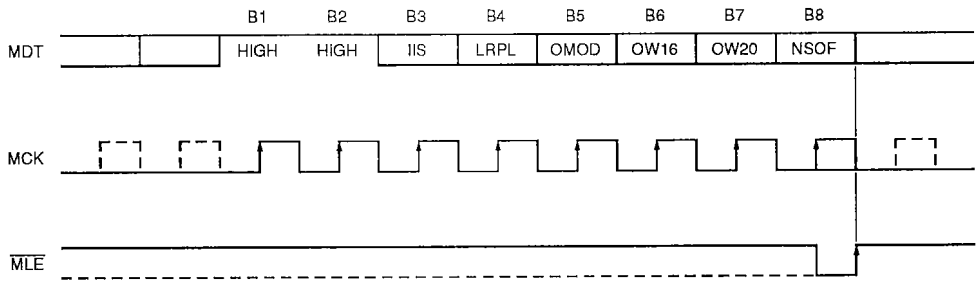


Figure 4. Mode flag setting 2

Table 2. Mode flag description

<table>
<tr><th rowspan="2">B1</th><th rowspan="2">B2</th><th rowspan="2">Bit</th><th rowspan="2">Mode flag</th><th colspan="3">Mode function select</th><th rowspan="2">Default at reset</th></tr>
<tr><th>Description</th><th>H/L</th><th>Function</th></tr>
<tr><td rowspan="12">HIGH</td><td rowspan="12">LOW</td><td rowspan="2">3</td><td rowspan="2">BILL</td><td rowspan="2">Bilingual output select</td><td rowspan="2"></td><td rowspan="2"><table><tr><th>BILL</th><th>BIRR</th><th>Output</th></tr><tr><td>LOW</td><td>LOW</td><td>Stereo</td></tr><tr><td>LOW</td><td>HIGH</td><td>RR</td></tr><tr><td>HIGH</td><td>LOW</td><td>LL</td></tr><tr><td>HIGH</td><td>HIGH</td><td>Stereo</td></tr></table></td><td rowspan="2">Stereo</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">BIRR</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">FSEL1</td><td rowspan="4">Deemphasis filter sampling frequency</td><td rowspan="4"></td><td rowspan="4"><table><tr><th>FSEL1</th><th>FSEL2</th><th>Frequency</th></tr><tr><td>LOW</td><td>LOW</td><td>44.1 kHz</td></tr><tr><td>LOW</td><td>HIGH</td><td>48.0 kHz</td></tr><tr><td>HIGH</td><td>LOW</td><td>44.1 kHz</td></tr><tr><td>HIGH</td><td>HIGH</td><td>32.0 kHz</td></tr></table></td><td rowspan="4">44.1 kHz</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">FSEL2</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">DEEM</td><td rowspan="2">Deemphasis select</td></tr>
<tr><td>LOW</td><td>Deemphasis OFF</td><td rowspan="2">OFF</td></tr>
<tr><td>HIGH</td><td>Deemphasis ON</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">MUTE</td><td rowspan="2">Mute select</td></tr>
<tr><td>LOW</td><td>Mute OFF</td><td rowspan="2">OFF</td></tr>
<tr><td>HIGH</td><td>Mute ON</td></tr>
<tr><td rowspan="12">LOW</td><td rowspan="12">HIGH</td><td rowspan="2">3</td><td rowspan="2">IIS</td><td rowspan="2">Serial input format select</td></tr>
<tr><td>LOW</td><td>Normal serial input</td><td rowspan="2">Normal</td></tr>
<tr><td>HIGH</td><td>IIS serial input</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">LRPL</td><td rowspan="2">LRCI polarity</td></tr>
<tr><td>LOW</td><td>Left/right = HIGH/LOW</td><td rowspan="2">HIGH/LOW</td></tr>
<tr><td>HIGH</td><td>Left/right = LOW/HIGH</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">OMOD</td><td rowspan="2">Output mode</td></tr>
<tr><td>LOW</td><td>8fs L/R simultaneous</td><td rowspan="2">8fs L/R simultaneous</td></tr>
<tr><td>HIGH</td><td>4fs L/R alternating</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">OW16</td><td rowspan="4">Output bit word length select</td><td rowspan="4"></td><td rowspan="4"><table><tr><th>OW16</th><th>OW20</th><th>Output length</th></tr><tr><td>LOW</td><td>LOW</td><td>18-bit</td></tr><tr><td>LOW</td><td>HIGH</td><td>20-bit</td></tr><tr><td>HIGH</td><td>LOW</td><td>16-bit</td></tr><tr><td>HIGH</td><td>HIGH</td><td>18-bit</td></tr></table></td><td rowspan="4">18-bit</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">OW20</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">NSOF</td><td rowspan="2">Noise shaper select</td></tr>
<tr><td>LOW</td><td>Noise shaper ON</td><td rowspan="2">ON</td></tr>
<tr><td>HIGH</td><td>Noise shaper OFF</td></tr>
</table>

Audio Data Input (DIN, BCKI, LRCI, LRPL flags)

The input is in 16-bit, 2s-complement, MSB-first, serial data format.

The IIS flag selects the IIS serial input format. The SM5841A/B supports IIS-format data at frequencies above 32fs, including 64fs. Normal format is selected at system reset.

Input timing

Serial input data on DIN is clocked into an SIPO register on the rising edge of the BCKI bit clock, and then converted into parallel data.

The SIPO output data for each channel is latched into either the left-channel or right-channel input register on the rising/falling edge of LRCI.

The timing of the arithmetic and output circuits is independent of the input timing. Accordingly, phase differences between LRCI, BCKI and XTI do not cause incorrect operation, and data input clock jitter does not generate jitter in the output clock.

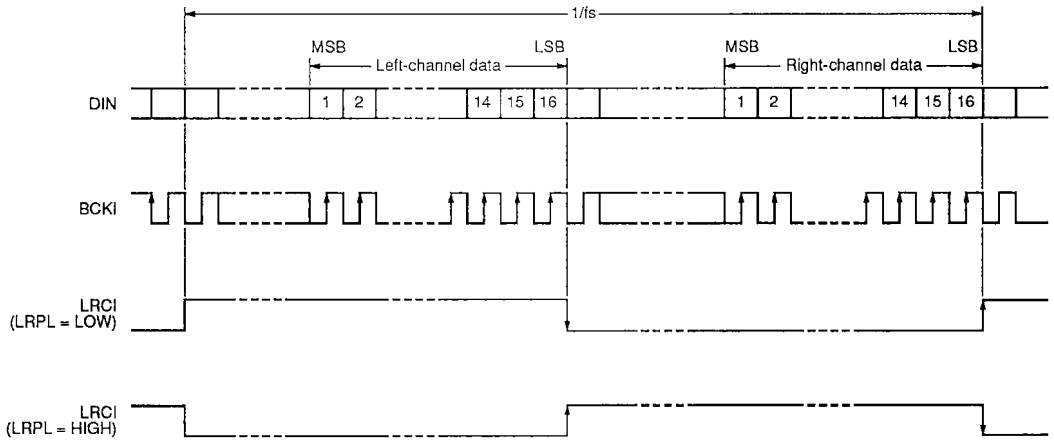


Figure 5. Normal data format (IIS = LOW)

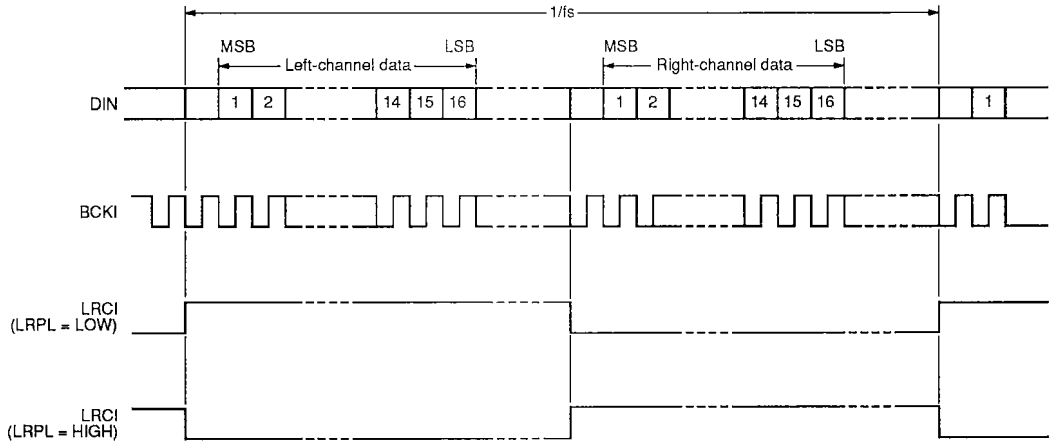


Figure 6. IIS data format (IIS = HIGH)

Data Output (DOL, DOR, BCKO, WCKO, DG, OMOD flag, OW16 flag, OW20 flag)

The output is in 2s-complement, MSB-first serial format. The output word length is 16-, 18- or 20-bit selectable using the OW16 and OW20 mode flags. 18-bit format is selected at system reset.

Filter arithmetic data has DC offset compensation added (SM5841B only) to reduce D/A converter zero-crossing distortion for very-small input signals. The offset correction added is approximately 0.8%.

- 512 LSB for 16-bit output
- 2048 LSB for 18-bit output
- 8192 LSB for 20-bit output

The BILL and BIRR flags select the output mode—LL, RR or stereo. LL (and RR) are mono modes where both channels output the left-channel (right-channel) signal. Stereo is selected at reset.

The output timing mode is selected by the OMOD flag. 8fs simultaneous left/right output and 4fs alternating left/right output are supported. 8fs simultaneous is selected at system reset.

Left- and right-channel data is output serially on either two pins (simultaneous or parallel channels) or one pin (alternating or serial channels), selected as shown in table 3.

Table 3. Output timing

Parameter	Symbol	System clock select	Output mode	
			8fs L/R simultaneous	4fs L/R alternating
Bit clock rate	t_B	$\overline{CKSL}$ = HIGH	1/192fs	1/192fs
		$\overline{CKSL}$ = LOW	1/256fs	1/256fs
Data word length	t_{DW}	$\overline{CKSL}$ = HIGH	$24t_B$	$24t_B$
		$\overline{CKSL}$ = LOW	$32t_B$	$32t_B$

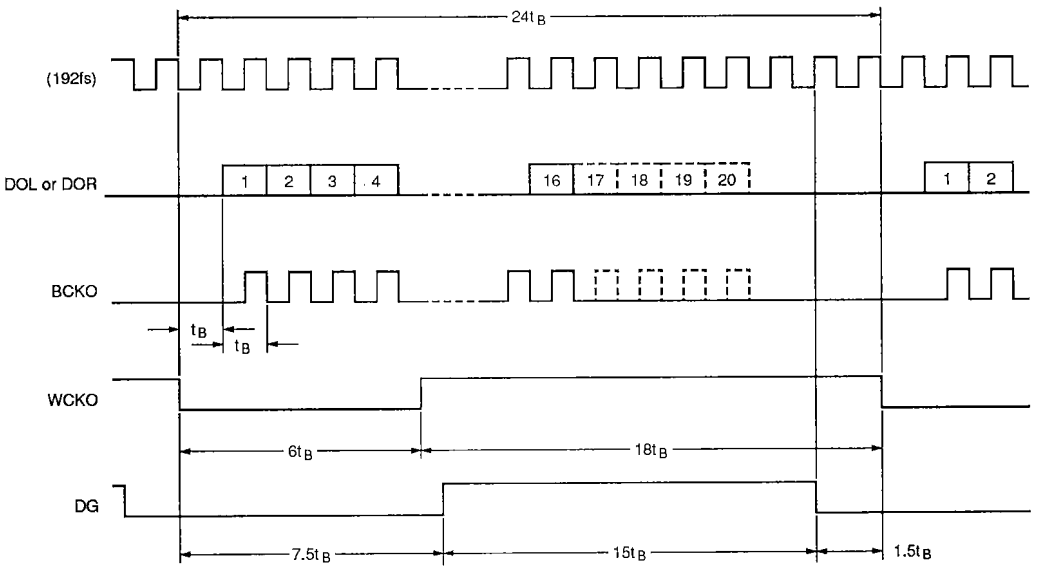


Figure 7. 8fs data output timing (OMOD = LOW, $\overline{CKSL}$ = HIGH)

Note

In 18-bit mode, pulses 17 and 18 are output, and in 20-bit mode, pulses 17 to 20 are output.

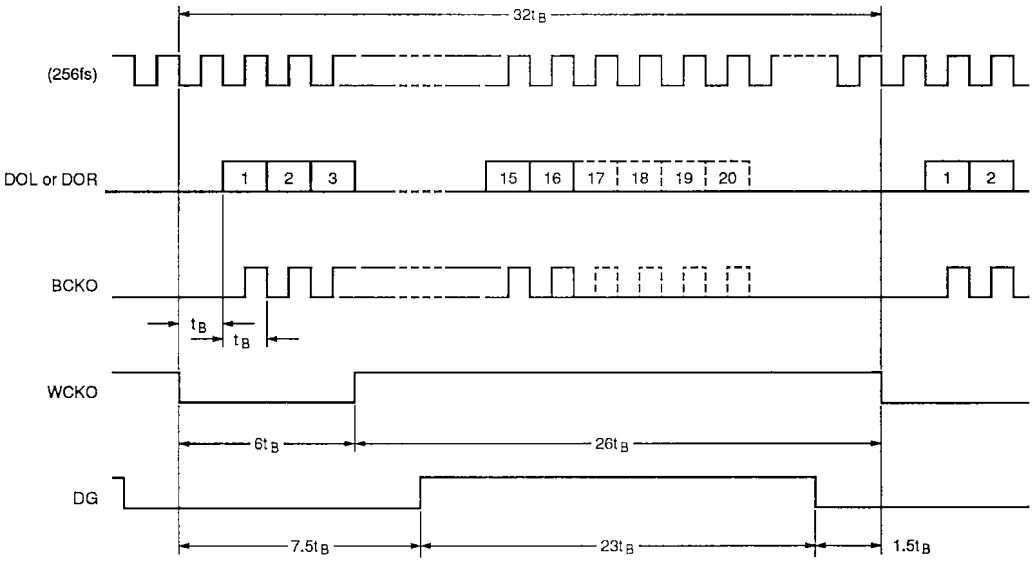


Figure 8. 8fs data output timing (OMOD = LOW, $\overline{\text{CKSL}}$ = LOW)

Note

In 18-bit mode, pulses 17 and 18 are output, and in 20-bit mode, pulses 17 to 20 are output.

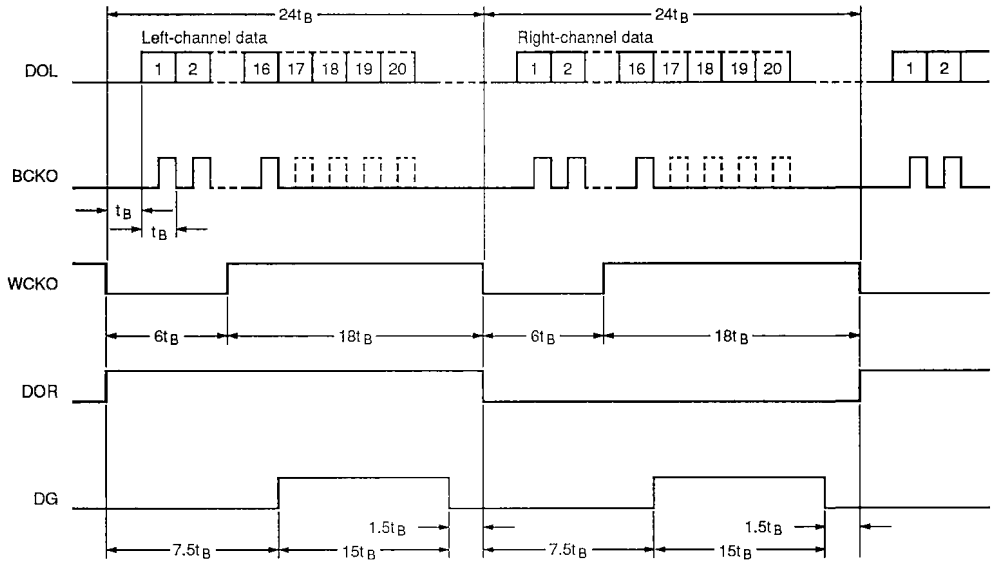


Figure 9. 4fs data output timing (OMOD = HIGH, $\overline{\text{CKSL}}$ = HIGH)

Note

In 18-bit mode, pulses 17 and 18 are output, and in 20-bit mode, pulses 17 to 20 are output.

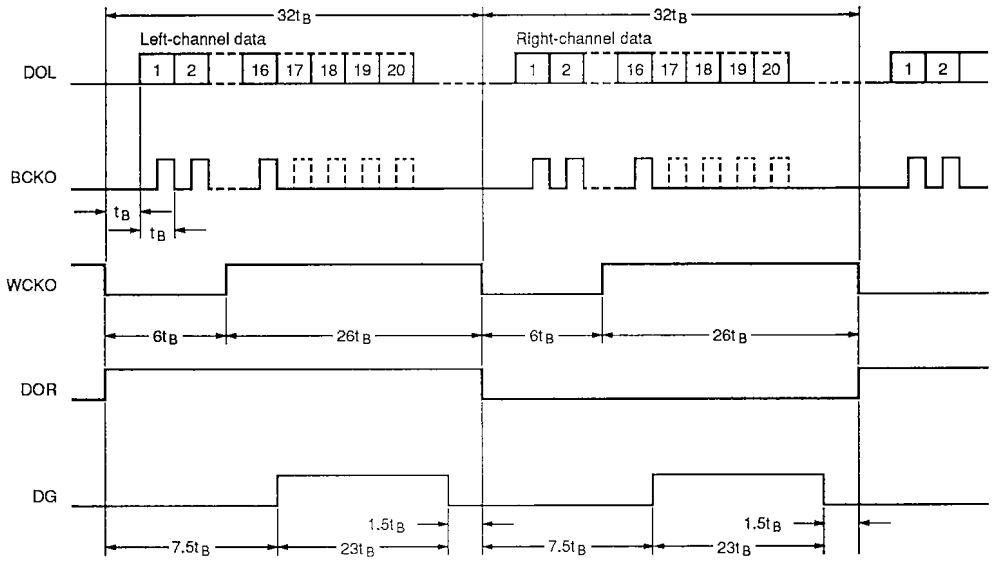


Figure 10. 4fs data output timing (OMOD = high, $\overline{CKSL}$ = LOW)

Note

In 18-bit mode, pulses 17 and 18 are output, and in 20-bit mode, pulses 17 to 20 are output.

System Reset

The SM5841A/B must be reset at power-ON by applying at LOW-level pulse on $\overline{RST}$.

The following conditions occur at system reset.

1. The arithmetic and output timing counters are reset on the next LRCI start edge after XTI has stablilized.
2. All data flags are reset to LOW when $\overline{RST}$ goes HIGH.
3. Mute attenuation is reset to OFF when $\overline{RST}$ goes HIGH.

A power-ON reset pulse can be applied from a controlling microprocessor, or by connecting a 300 pF capacitor between $\overline{RST}$ and VSS for systems where XTI and LRCI stablilize simultaneously. For others systems that do not use a microcontroller, XTI and LRCI must stabilize before $\overline{RST}$ goes HIGH. A larger capacitor can be used to ensure that this occurs.

If the system clock becomes corrupted or develops jitter such that the timing increases above ±3/8 × (LRCI clock frequency), then the internal timing will automatically reset on the next LRCI start edge. This timing re-synchronization can generate an output click noise.

Output Muting

When $\overline{RST}$ goes LOW, DOL and DOR go LOW, immediately muting the output words. Muting is released and timing re-synchronized on the third LRCI rising edge after $\overline{RST}$ goes HIGH. The BCKO and WCKO clock outputs do not stop.

Furthermore, when $\overline{CKSL}$ changes state, LRPL changes state or the internal timing re-synchronizes, as shown in figure 11, and output muting and release occurs just as when $\overline{RST}$ goes LOW.

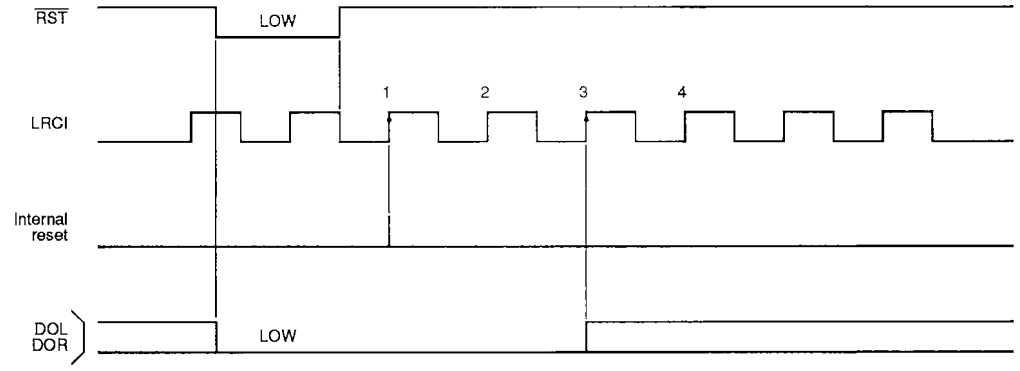


Figure 11. System reset timing and output muting

TIMING DIAGRAMS

Input Timing (DIN, BCKI, LRCI)

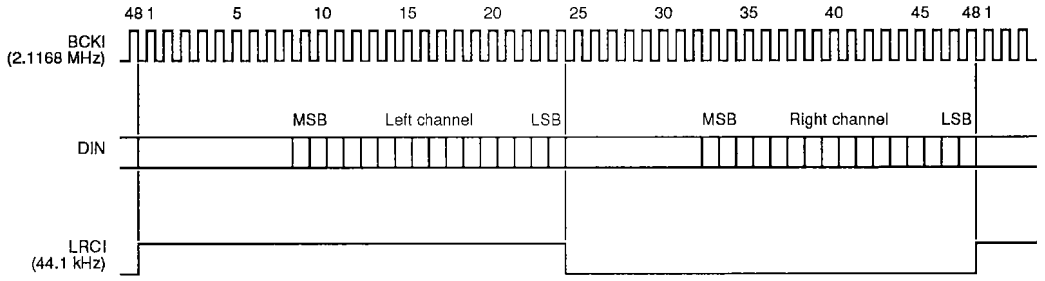


Figure 12. Input timing 1 (IIS = LOW, LRPL = LOW)

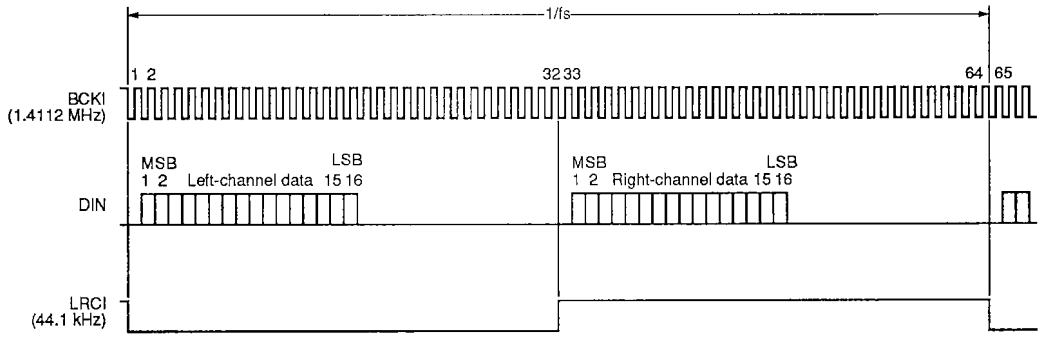


Figure 13. Input timing 2 (IIS = HIGH, LRPL = HIGH)

Output Timing (DOL, DOR, BCKO, WCKO, DG)

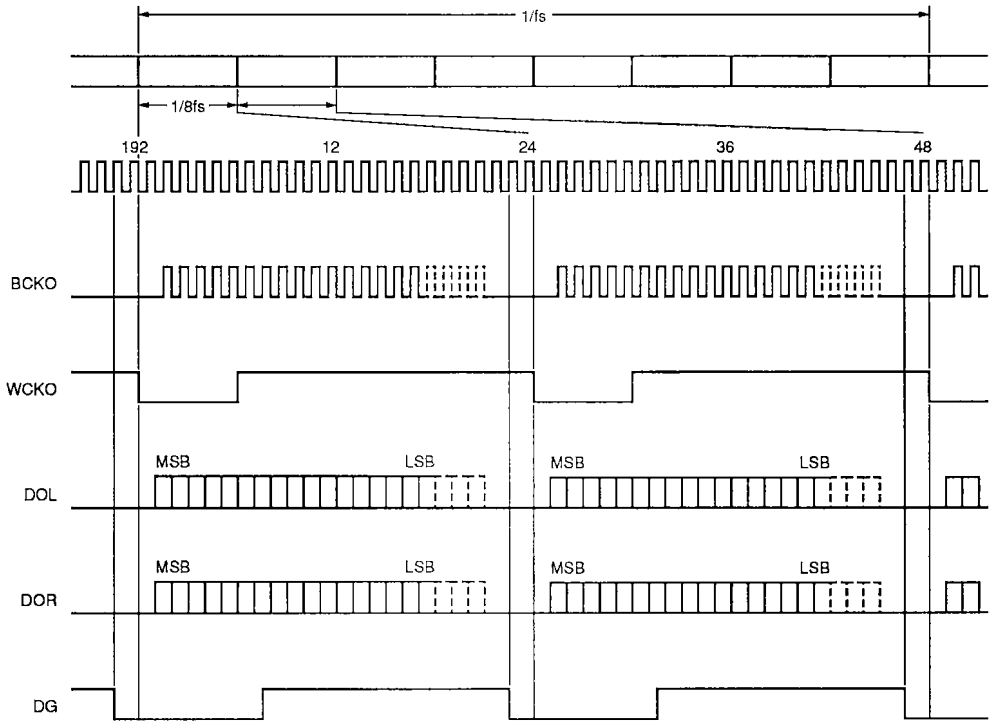


Figure 14. 8fs output timing 1 ($\overline{\text{CKSL}}$ = HIGH, OMOD = LOW)

Note
In 18-bit mode, pulses 17 and 18 are output, and in 20-bit mode, pulses 17 to 20 are output.

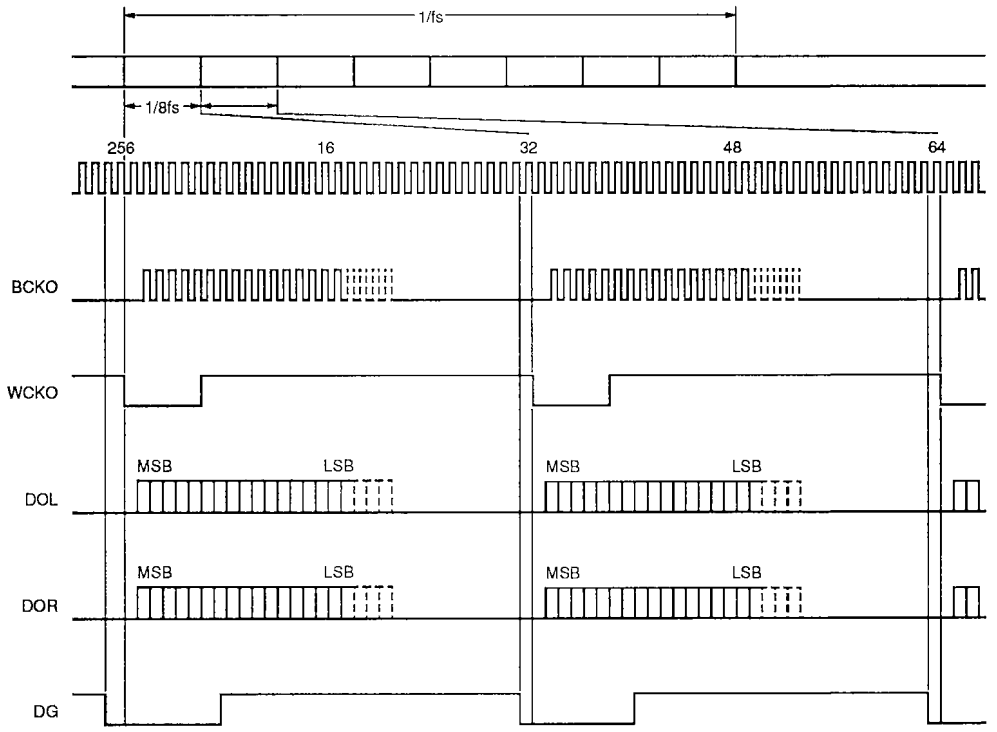


Figure 15. 8fs output timing 2 ($\overline{\text{CKSL}}$ = LOW, OMOD = LOW)

Note
In 18-bit mode, pulses 17 and 18 are output, and in 20-bit mode, pulses 17 to 20 are output.

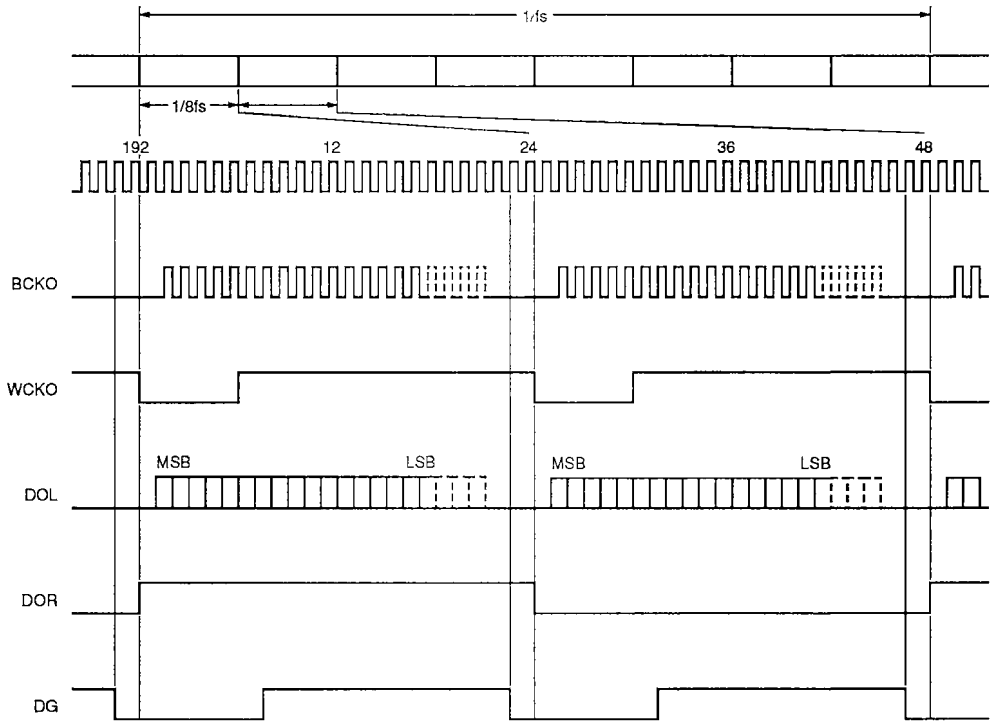


Figure 16. 4fs output timing 1 ($\overline{\text{CKSL}}$ = HIGH, OMOD = HIGH)

Note
In 18-bit mode, pulses 17 and 18 are output, and in 20-bit mode, pulses 17 to 20 are output.

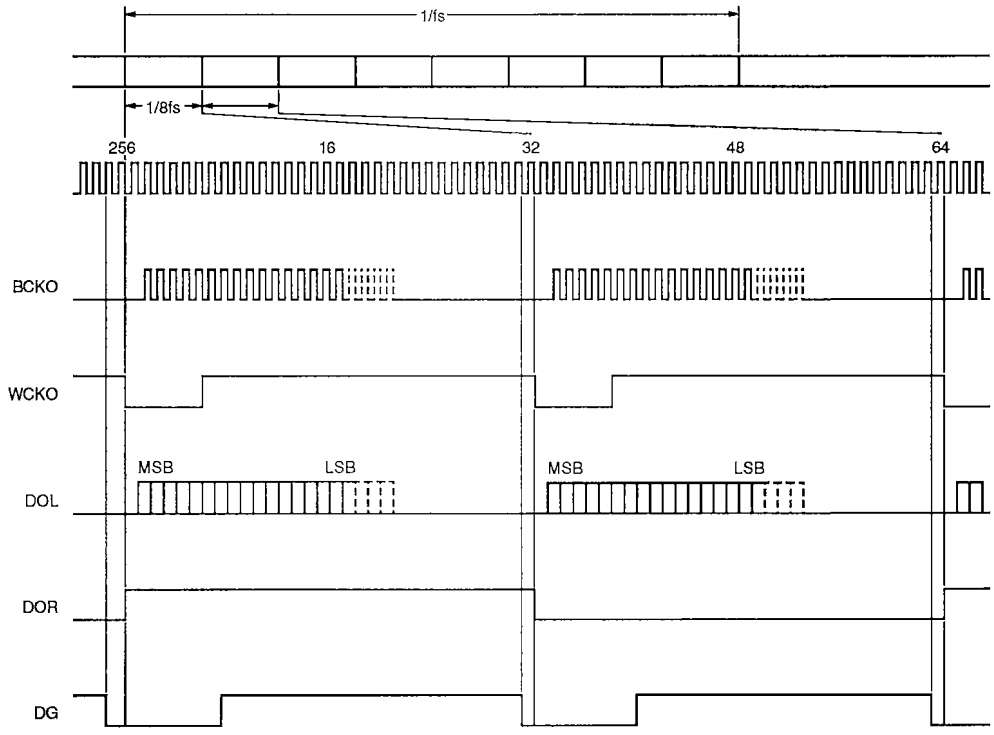
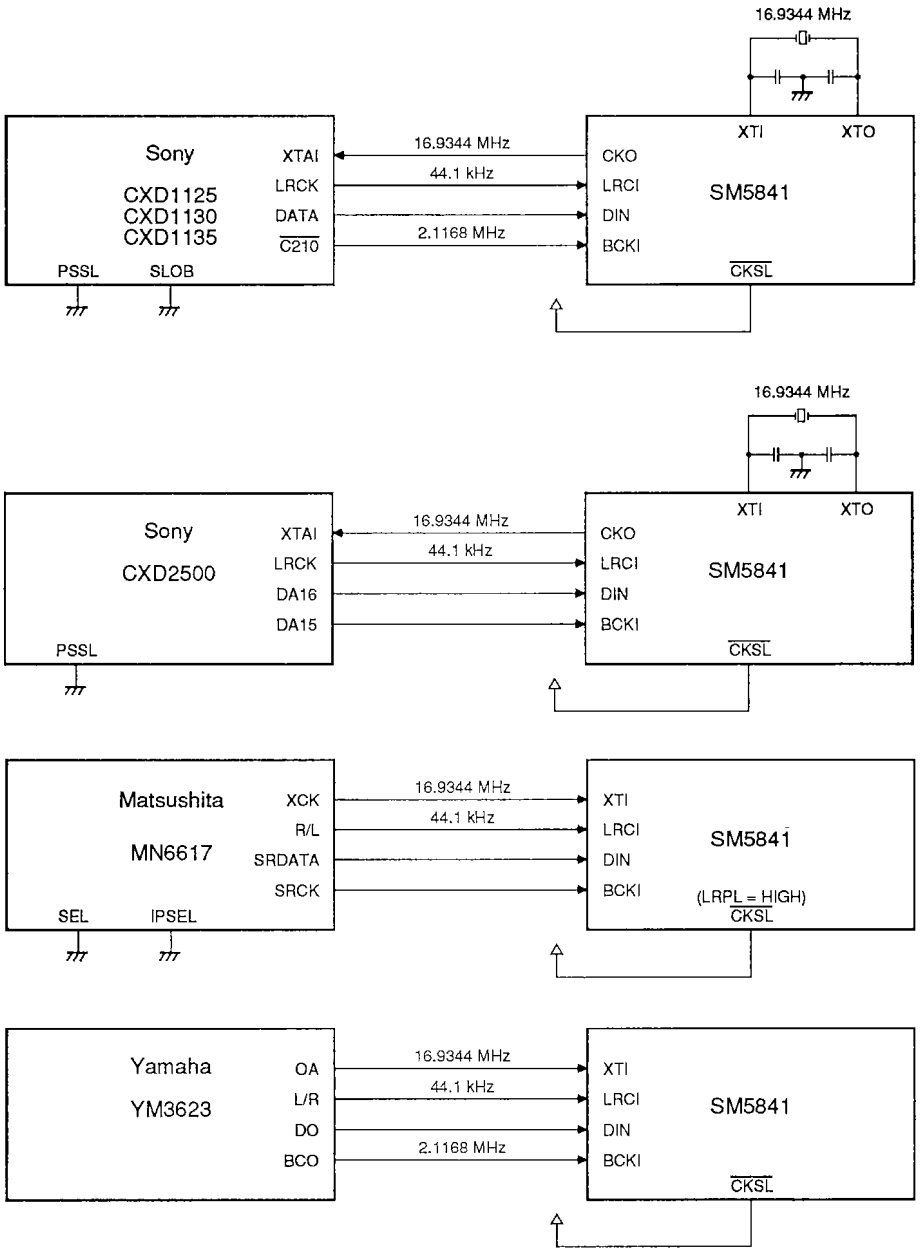


Figure 17. 4fs output timing 2 ($\overline{\text{CKSL}}$ = LOW, OMOD = HIGH)

Note
In 18-bit mode, pulses 17 and 18 are output, and in 20-bit mode, pulses 17 to 20 are output.

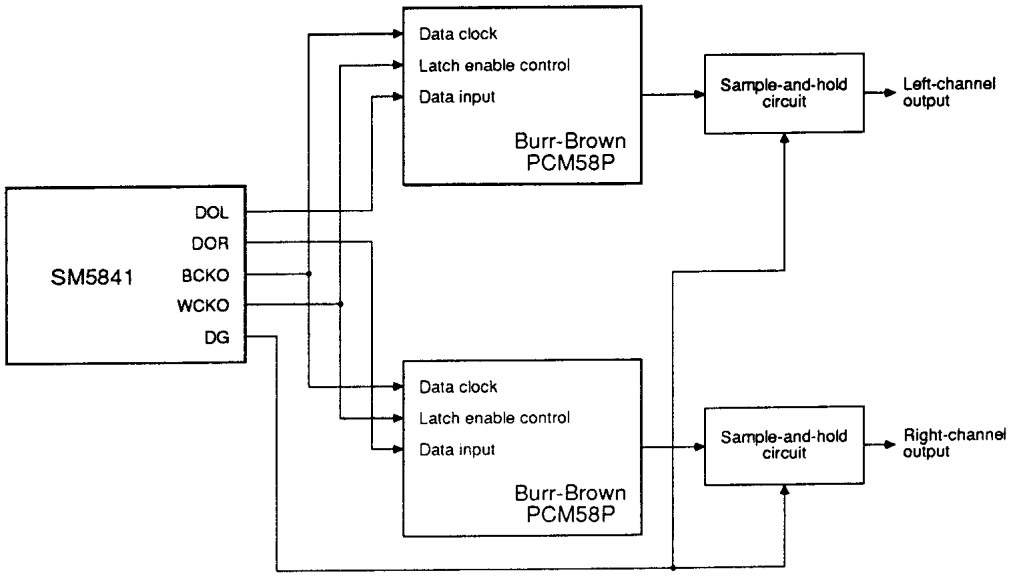
APPLICATION CIRCUITS

Input Interface Circuits

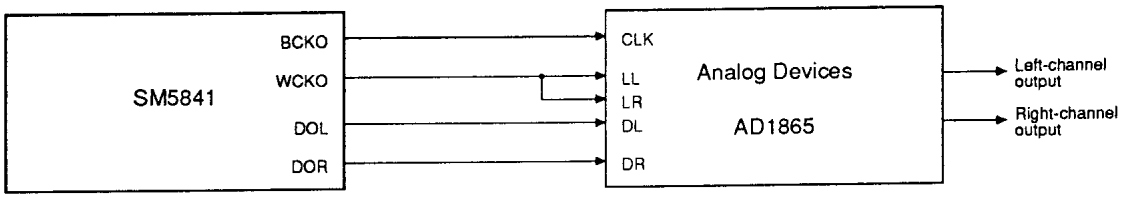


Output Interface Circuits

18-bit dual D/A converter (8fs L/R simultaneous output mode)



18-bit D/A converter



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NC9251BE 1998.10